DDR2/DDR3 Data Sheet

Features

The MCTL supports the following features:

- Compatible with JEDEC standard DDR2/DDR3 SDRAMs
- PHY Utility Block (PUB) – Automated RTL algorithms to ease PHY initialization and production test (for use with PUB-compatible DWC DDR3/2 PHYs)
- Uses a 4:1 data width conversion (also known as X4) from host interface to DDR*n*
- Supports data rates of up to 2133Mb/s using 533MHz MCTL clock Up to 32 host ports using Host Memory Interface (HMI) or AMBA 3 AXI/AHB Separate configuration port using Controller Register Interface (CRI) or AMBA 3 AXI with independent clocking
- Compatibility with the AMBA 3 AXI protocol
- AXI data bus widths are four times the DDR data bus widths
- Selectable close bank policy (auto-precharge at burst conclusion)
- Variable burst lengths independent of the programmed DDR SDRAM burst length
- Support for all AXI burst types: fixed, incremental, and wrap AXI clock asynchronous/synchronous to the MCTL clock
- Operation with full AXI data width even when DDR data bus is programmed for half data width
- Accommodates standard industry SDRAM widths and depths
- Support for connection to industry standard UDIMMs (Unbuffered DIMMs) and RDIMMs (Registered DIMMs)
- Programmable timing parameters support DDR2/DDR3 SDRAM components from various vendors
- Extended register fields to permit interfacing to non-standard devices
- Advanced DDR2/DDR3 features such as ODT and additive latency
- Compensation for board delays and variable latencies through programmable pipelines
- Up to four external memory ranks
- Advanced command re-ordering and scheduling to maximize bus utilization
- Low power modes, such as power-down and self-refresh for DDR2/DDR3 SDRAM Automatic SDRAM refresh control including adjustable parameters Programmable ultra-high priority port (port 0), typically a CPU port
- Configurable per-command priority with up to eight priority levels; also serves as a per-port priority
- Programmable priority arbitration and anti-starvation mechanisms
- Secondary round-robin host port arbitration with programmable (per-port) number of commands serviced per arbitration from each port
- Configurable and programmable address mapping, including bypass option to support external address mapping
- Comprehensive verification environment for quick ramp-up and integration

Availability

- Q4, 2010

*To obtain more information about the DDR2/DDR3 or other C*Core™ products, please contact the C*Core Technology Co., Ltd. by phone: 0512-68091375, email: support@china-core.com or web: http://www.china-core.com.*

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